

FIG.1

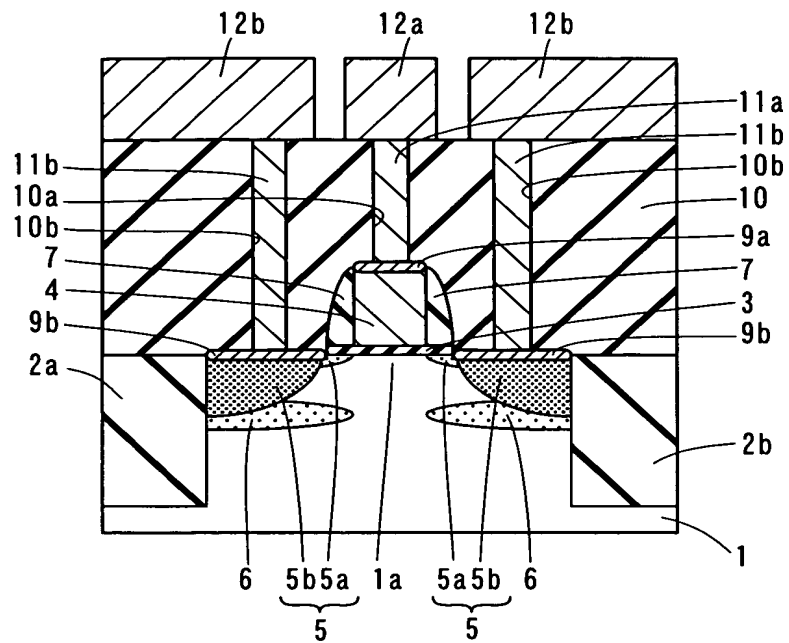


FIG.2

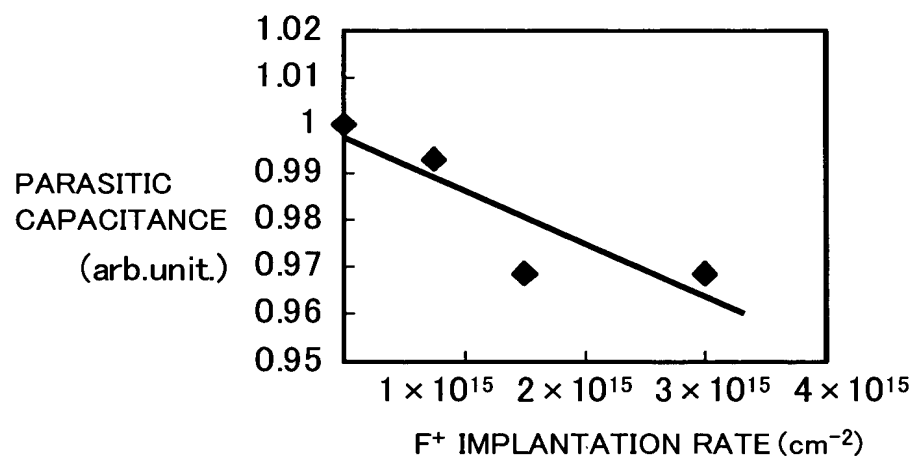


FIG.3

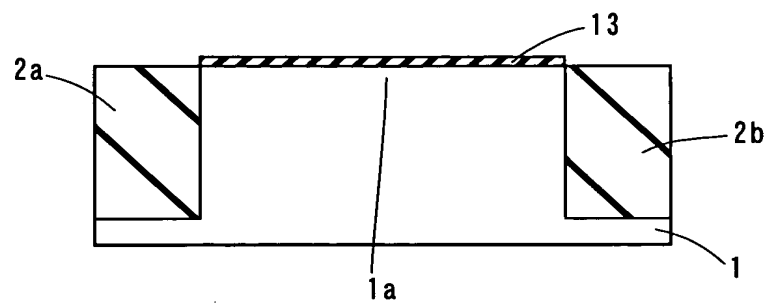


FIG.4

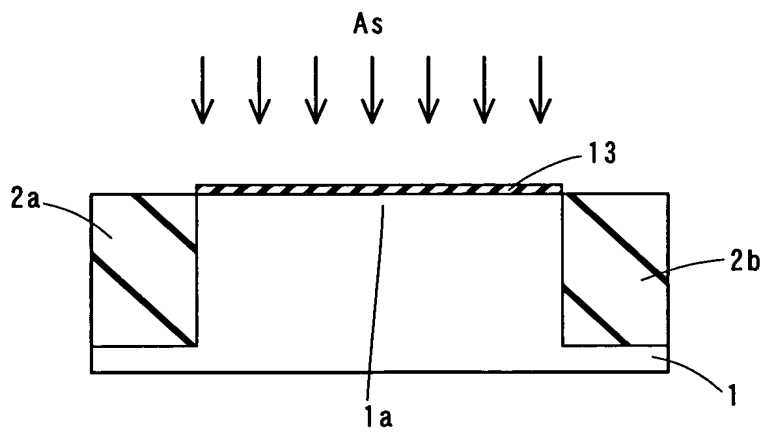


FIG.5

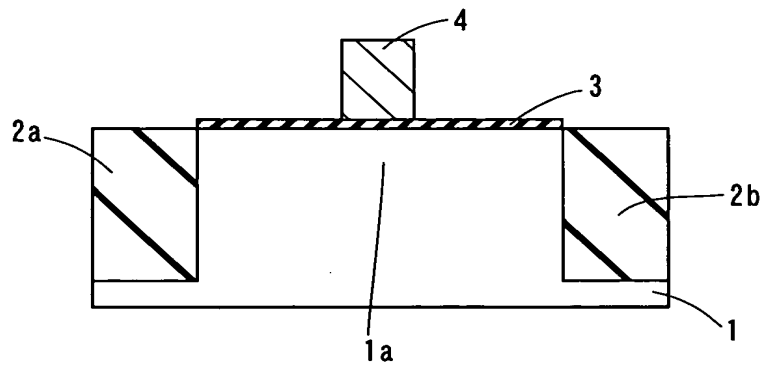


FIG.6

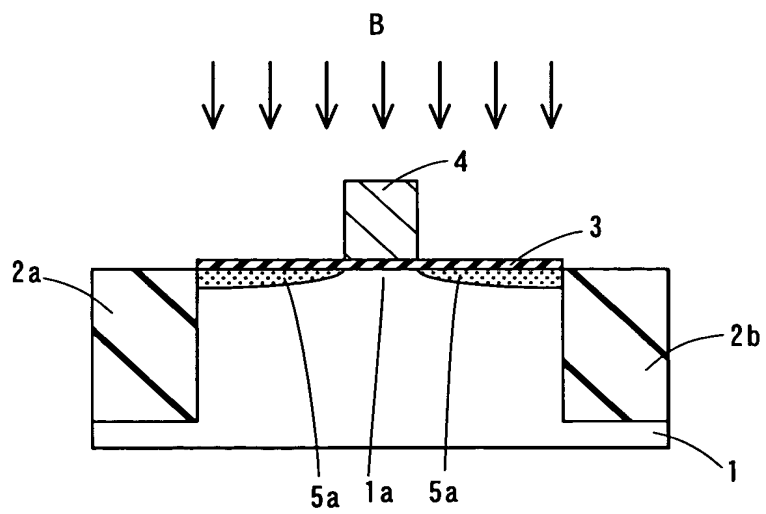


FIG.7

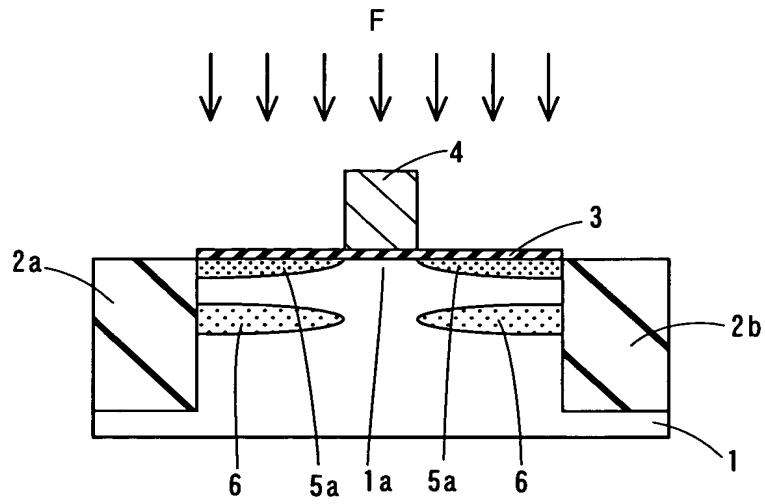
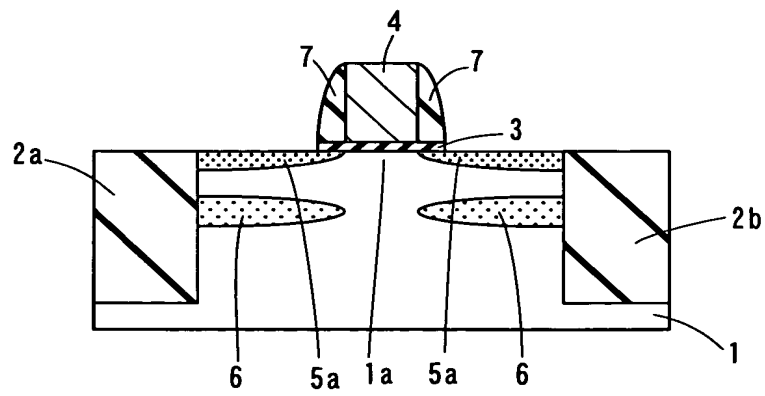


FIG.8



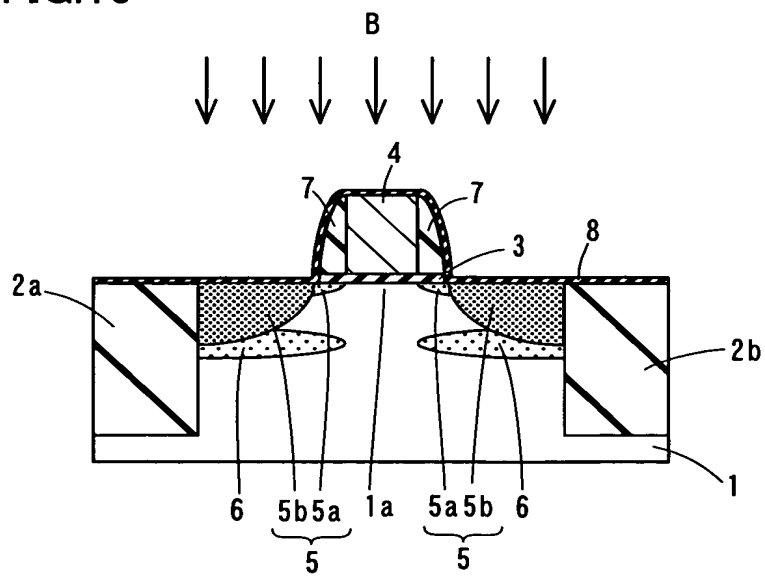
[illegible]

FIG.11

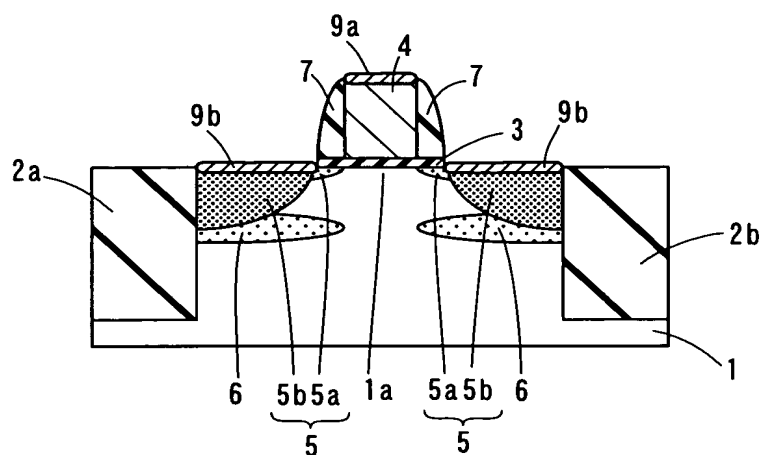
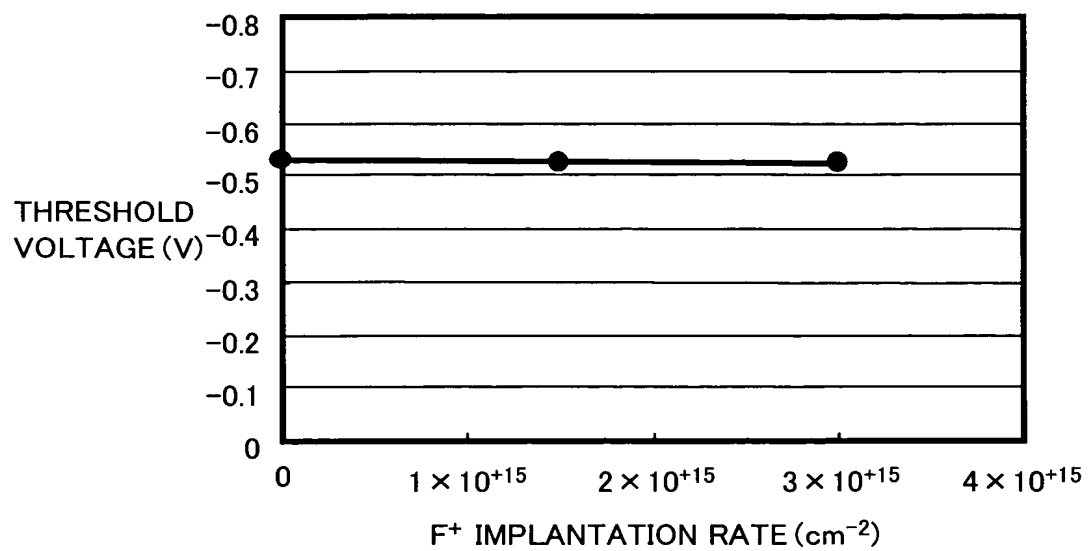


FIG.12



This cross-sectional view shows a substrate 21 with a trench 22. The trench 22 is divided into three sections: 22a, 22b, and 22c. The trench 22 is filled with a material 36, which is shown with diagonal hatching. The material 36 is also present in the trench 22b. The trench 22 is formed in the substrate 21.

FIG.15

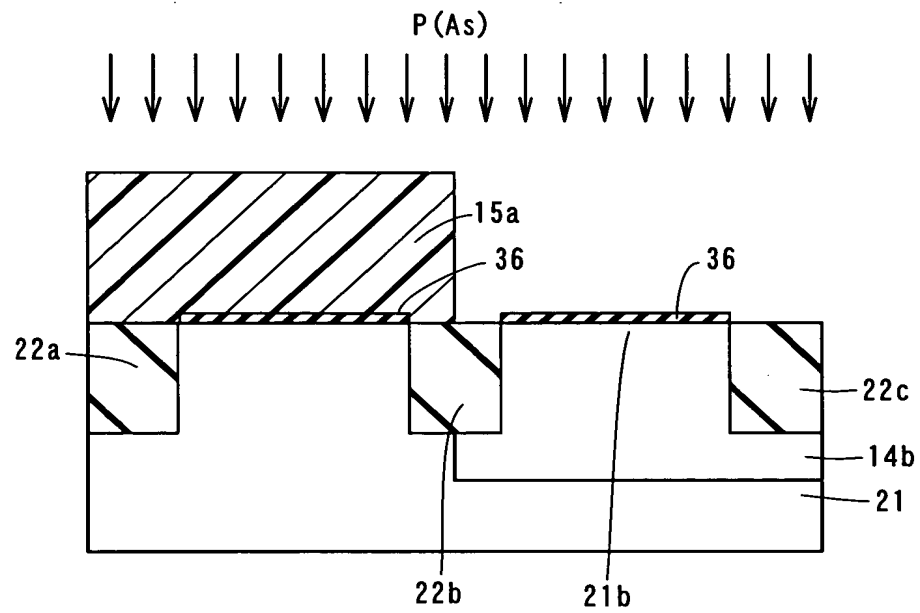


FIG.16

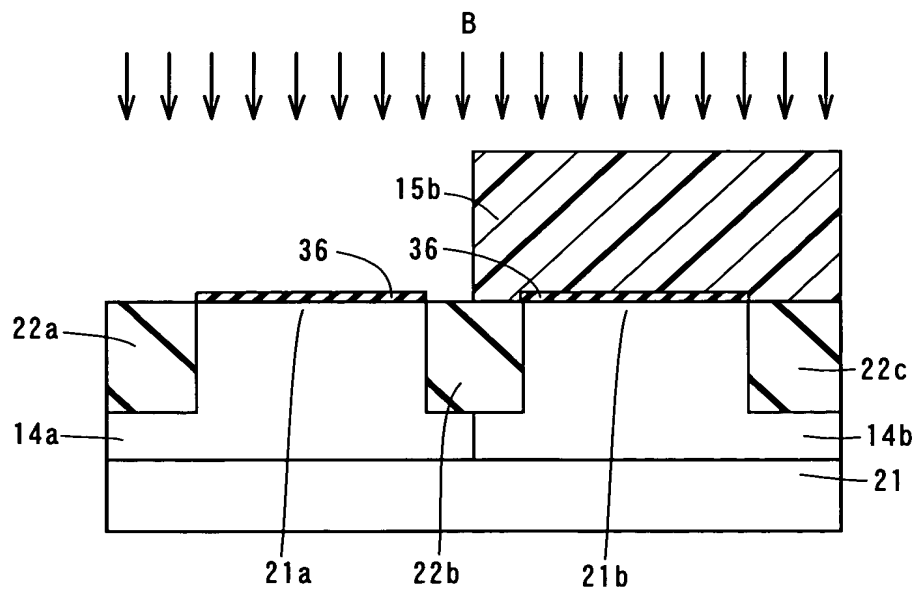




FIG.17

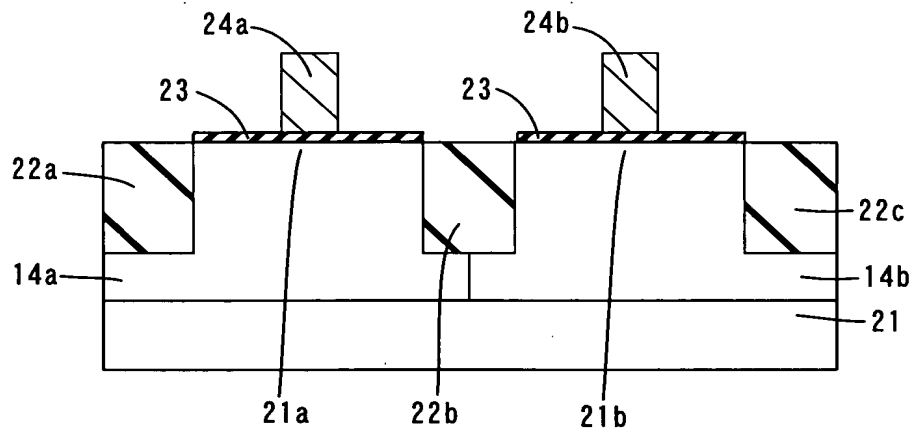


FIG.18

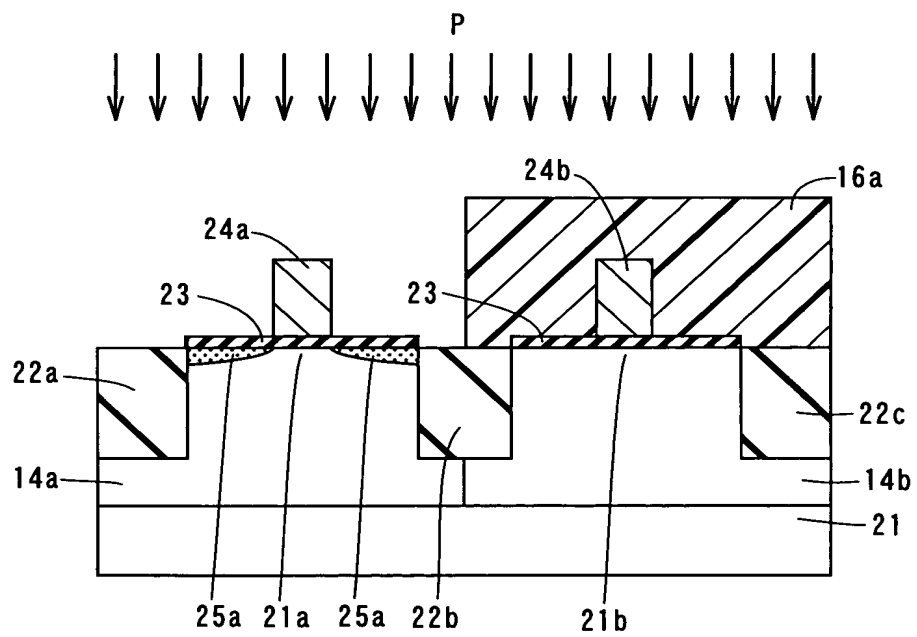


FIG.19

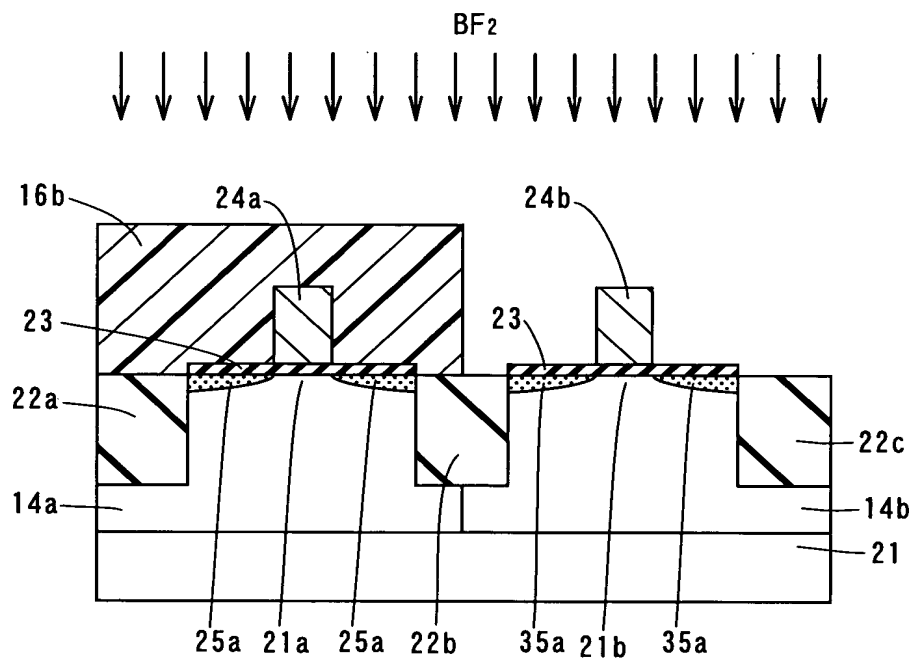


FIG.20

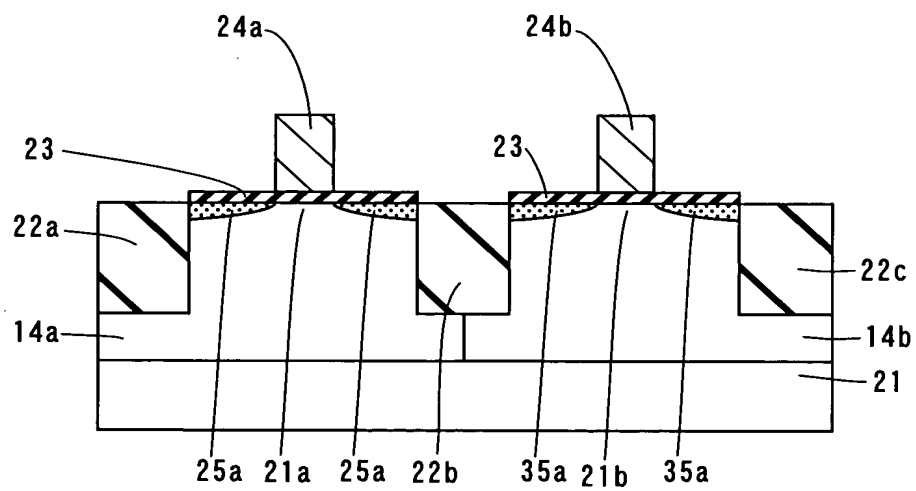


FIG.21

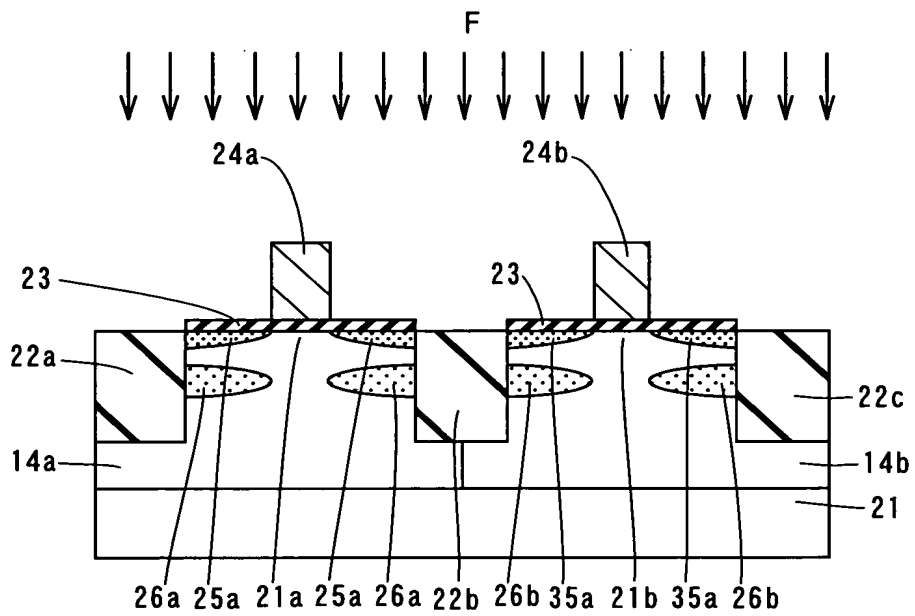
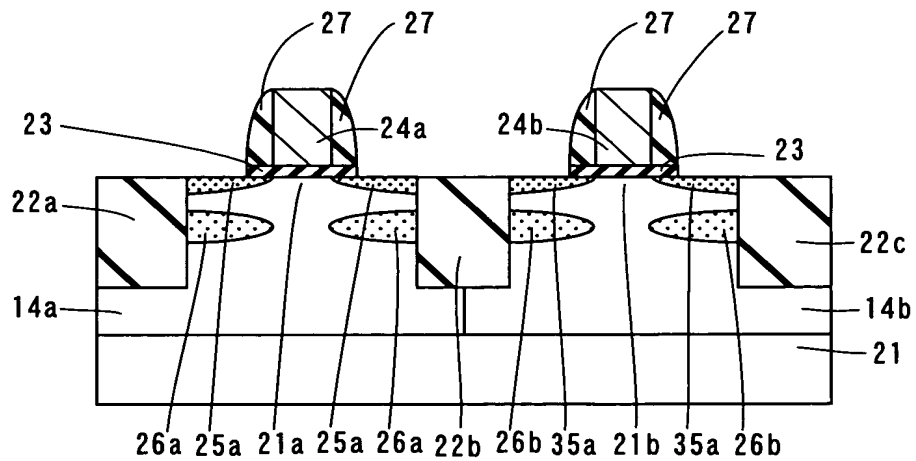


FIG.22



This diagram shows a cross-sectional view of a semiconductor device with two gate structures. The device consists of a substrate 21, a base layer 14a, and a gate layer 22a. The gate structures are formed by a gate oxide layer 23, a gate electrode 27, and a gate spacer 24a. The gate structures are separated by a channel region 26a. The device is also shown with a second gate structure 24b and a channel region 26b. The gate structures are formed by a gate oxide layer 23, a gate electrode 27, and a gate spacer 24b. The device is also shown with a second gate structure 24b and a channel region 26b. The gate structures are formed by a gate oxide layer 23, a gate electrode 27, and a gate spacer 24b. The device is also shown with a second gate structure 24b and a channel region 26b.

A cross-sectional view of a semiconductor device. At the top, a layer labeled 'As' is shown with downward-pointing arrows indicating an applied electric field. Below this, two transistors are depicted. Each transistor has a gate stack (27) on top of a gate dielectric (23). The gate dielectric is on a substrate (21). The transistors are separated by a channel stop (22a). The source and drain regions are labeled 24a and 24b. The substrate is labeled 21. Other labels include 14a, 14b, 17a, 17b, 22b, 22c, 25a, 25b, 26a, 26b, 35a, and 35b.

FIG.25

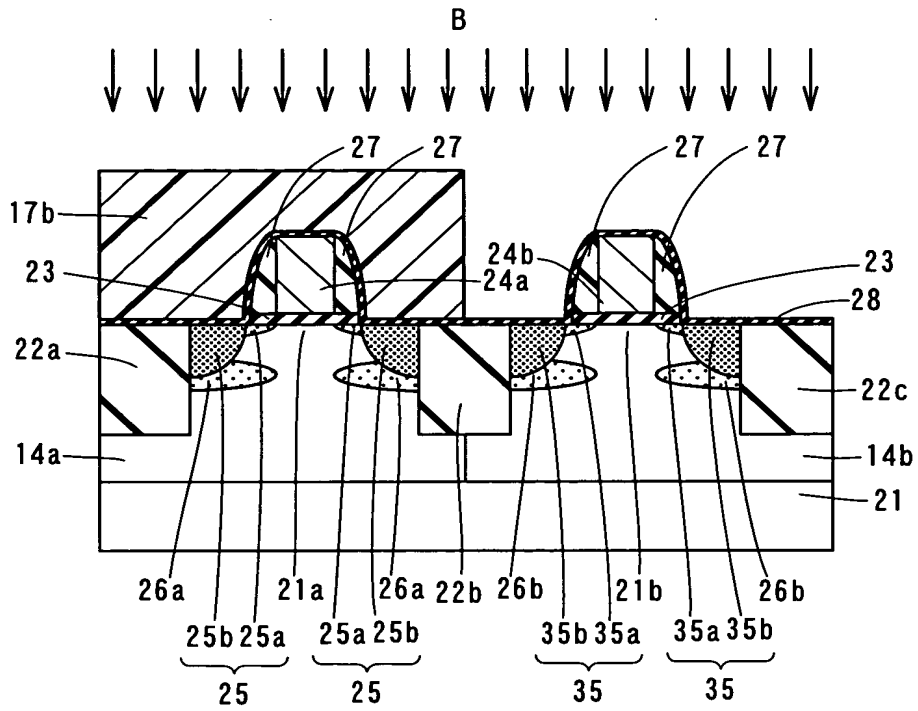


FIG.26

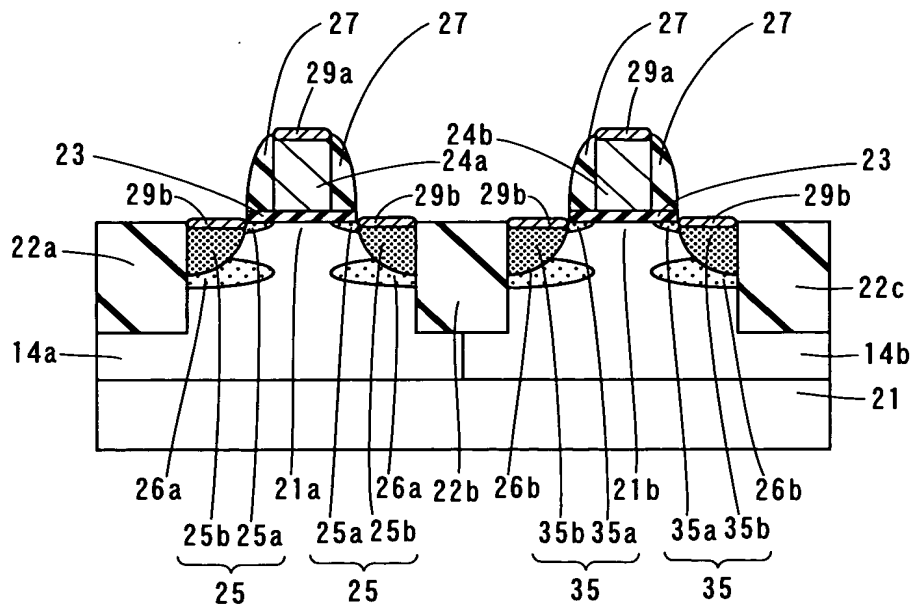


FIG.27

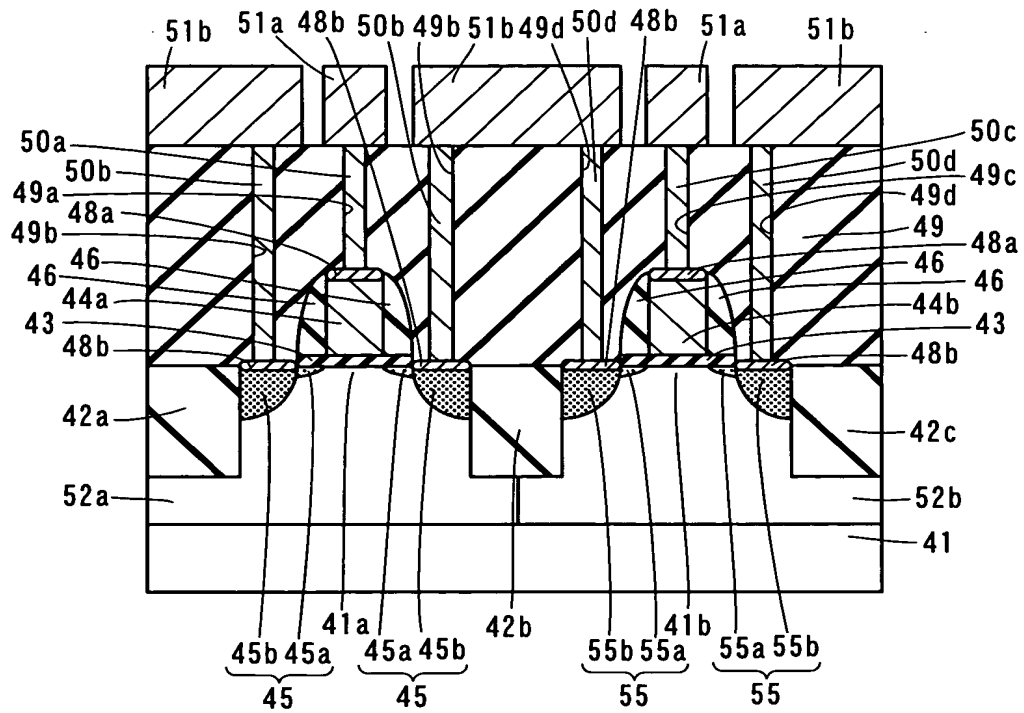


FIG.28

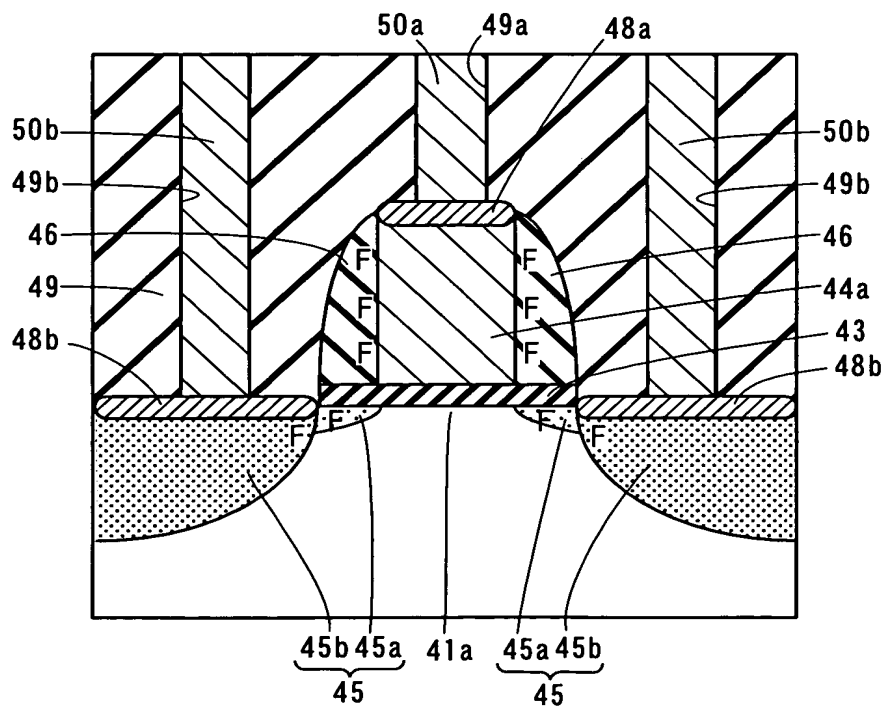


FIG.29

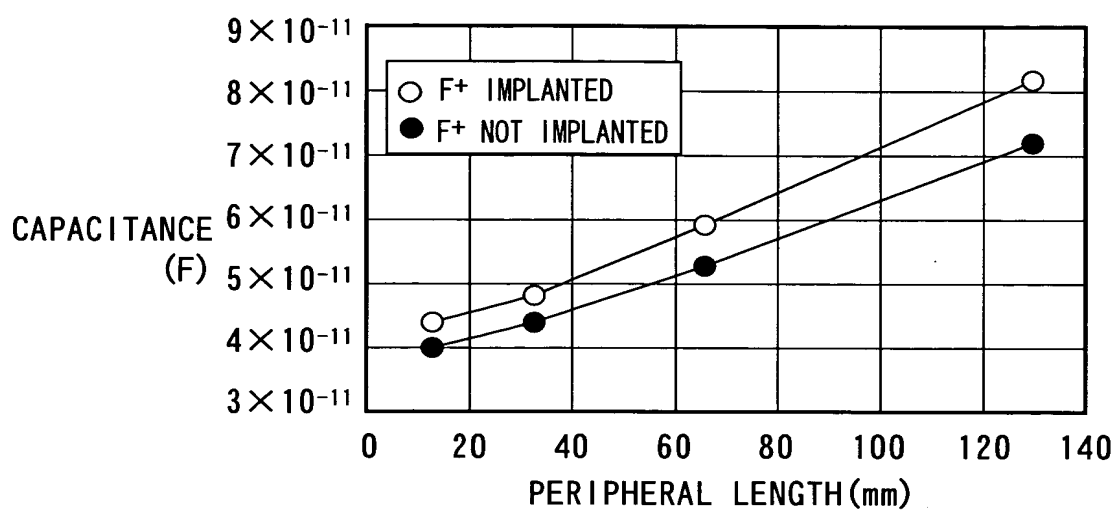
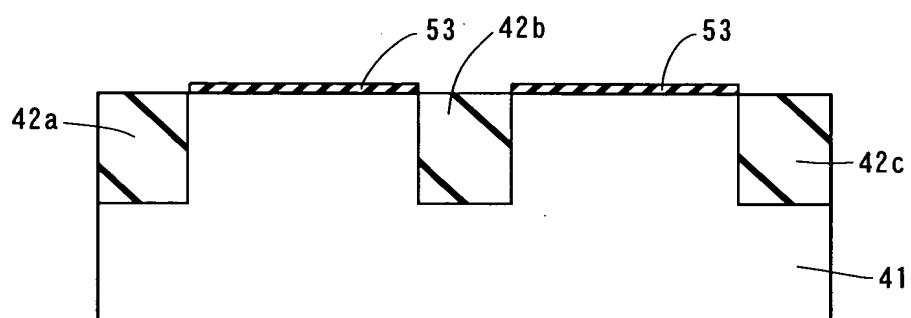


FIG.30



[illegible]

Fig. 1 is a cross-sectional view of a semiconductor device. It shows a substrate 41 with a thin layer 52a. A patterned layer 53 is on top of 52a, with regions 42a, 42b, and 42c. A thick layer 54b is on top of 53. Arrows B indicate a direction.



FIG.33

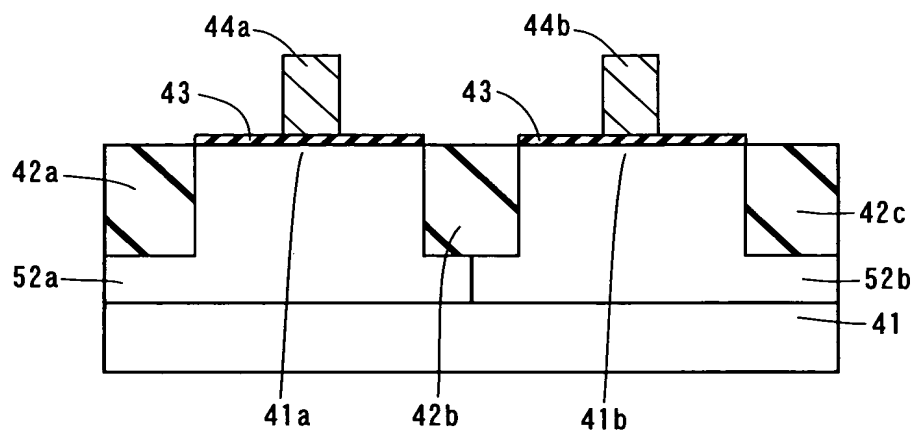


FIG.34

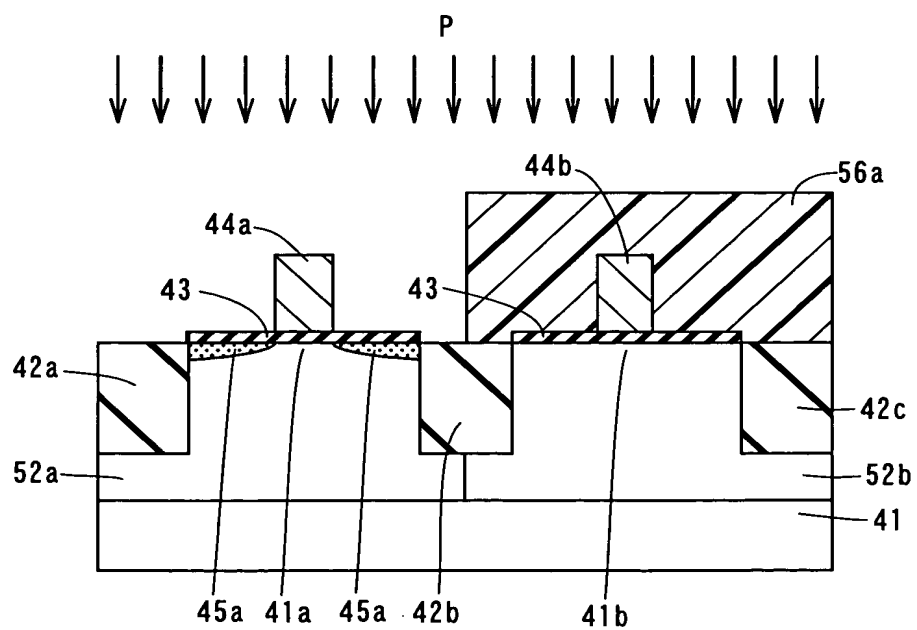


FIG.35

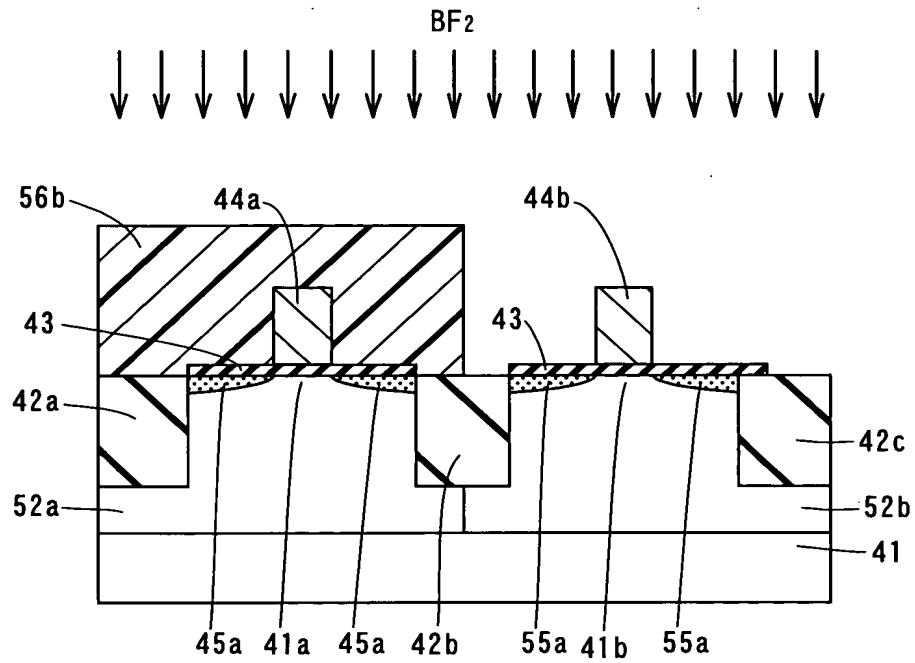


FIG.36

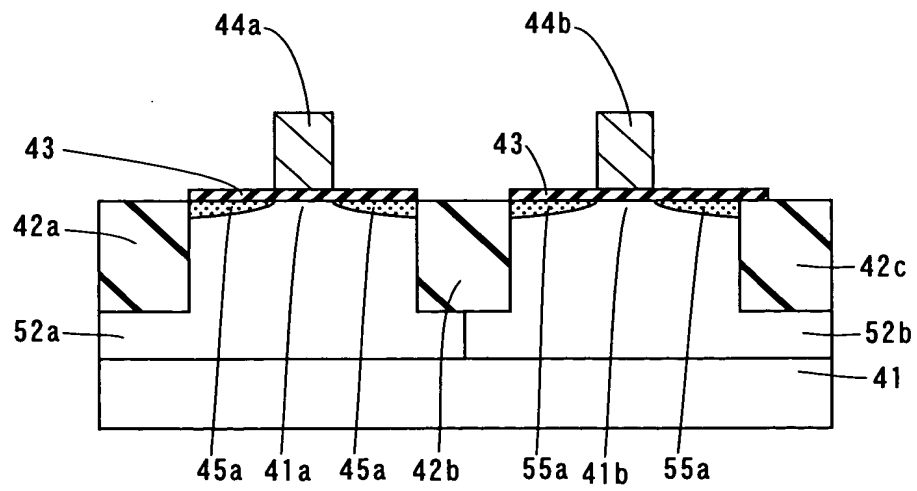


FIG.37

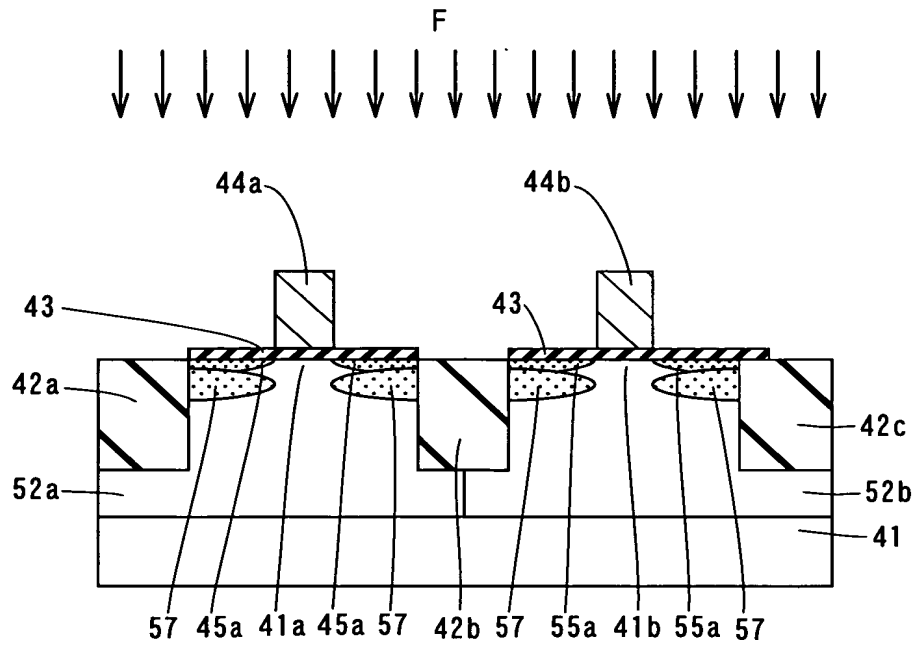
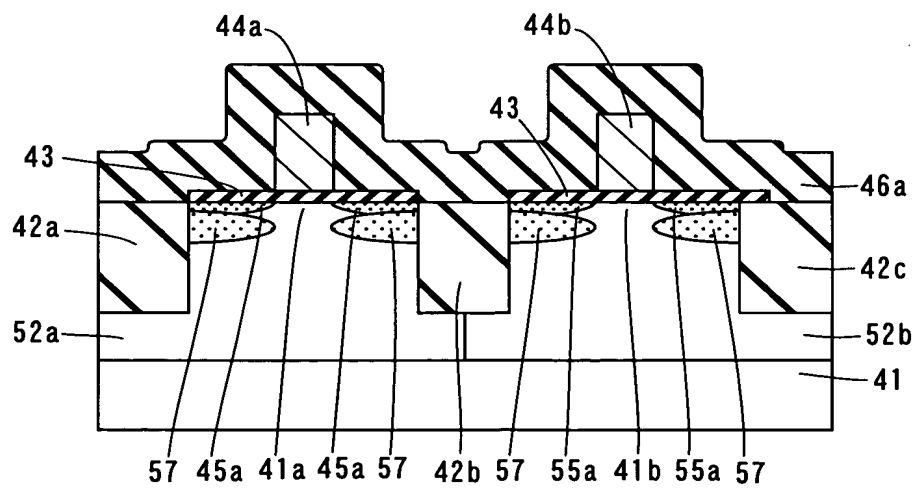


FIG.38



[illegible]

This cross-sectional view shows a semiconductor device with two gate structures. The substrate is labeled 41. A layer 52a is on top of the substrate. Two gate structures, 44a and 44b, are formed on top of layer 52a. Each gate structure consists of a gate stack 43 and a gate cap 46. The gate stack 43 is composed of a layer 42a and a layer 42c. The gate cap 46 is on top of the gate stack 43. The regions between the gate structures are labeled 41a and 41b. The regions under the gate structures are labeled 45a and 45b. The regions under the gate structures are also labeled 57. The regions under the gate structures are also labeled 55a and 55b. The regions under the gate structures are also labeled 42b.

A cross-sectional view of a semiconductor device. At the top, a layer labeled 'As' is shown with downward-pointing arrows indicating ion implantation. Below this is a gate stack consisting of a gate dielectric (46) and a gate electrode (43). Two transistors are formed on either side of the gate stack. The transistors have a channel region (41a, 41b) and source/drain regions (42a, 42b, 42c). The source/drain regions are doped with impurities (45a, 45b, 45c) and are covered by a protective layer (47). The device is built on a substrate (41). Other labels include 44a, 44b, 52a, 52b, 55a, 55b, 57, and 58a, which likely refer to specific layers or regions within the device structure.

This cross-sectional view shows two transistors on a substrate 41. The left transistor has a gate stack 43 on a gate insulator 58b, with a channel region 41a and source/drain regions 45a and 45b. The right transistor has a similar structure with gate stack 43, channel region 41b, and source/drain regions 55a and 55b. A central region 42b is located between the two transistors. The device is covered by a top layer 47, and a bottom layer 52b is present below the substrate 41. Arrows at the top indicate a downward force or pressure.

FIG.43

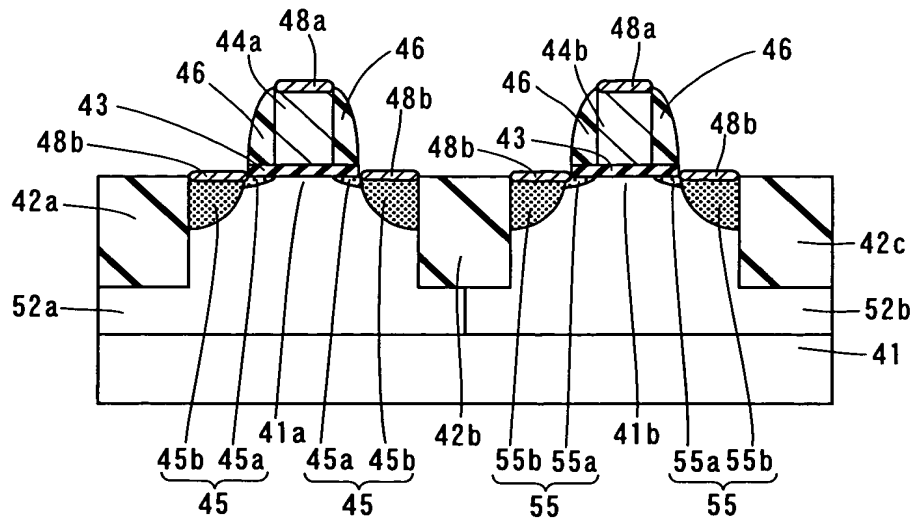


FIG.44

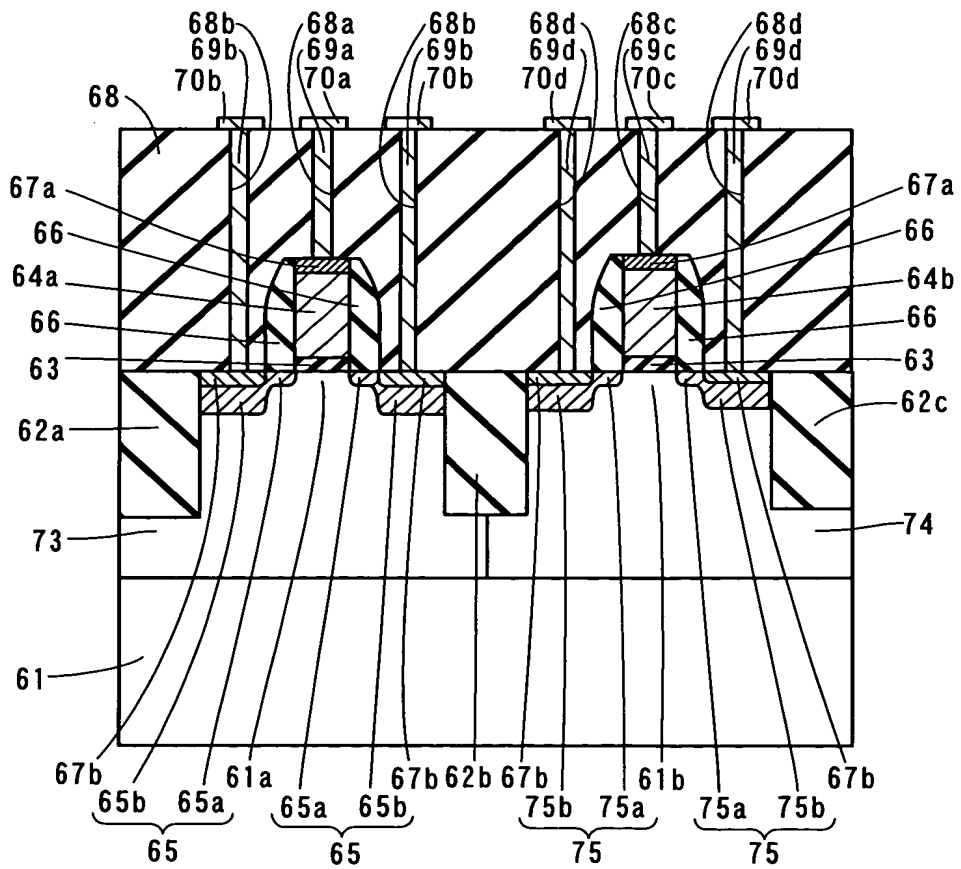


FIG.45

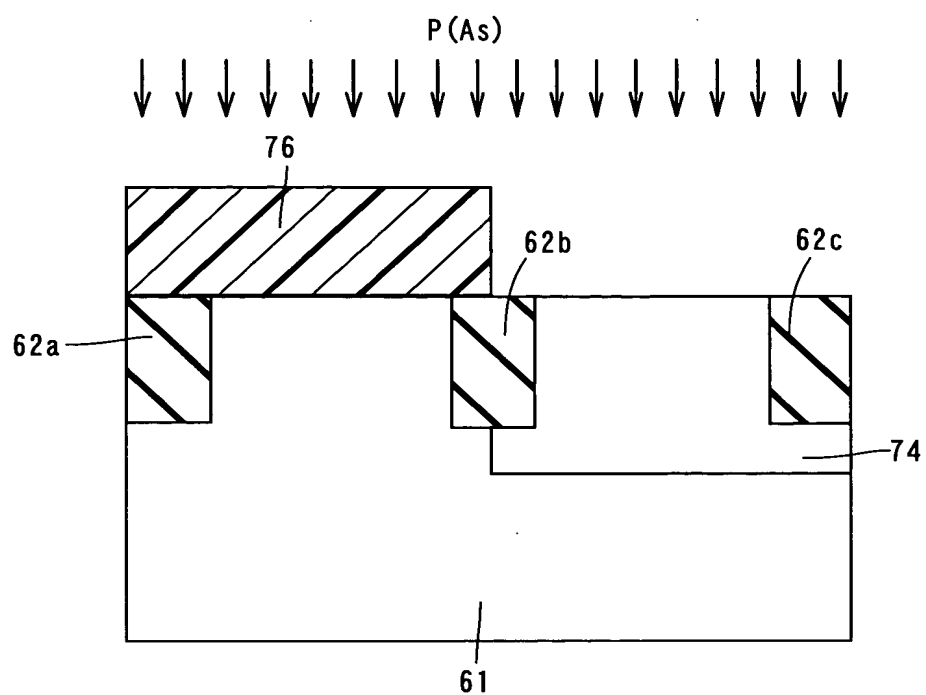


FIG.46

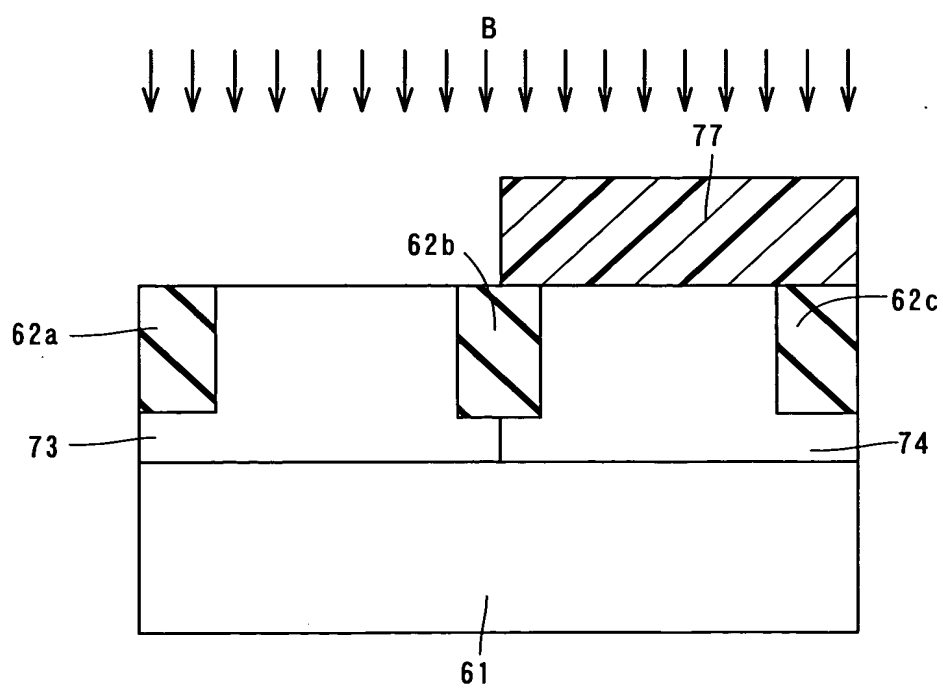


FIG.47

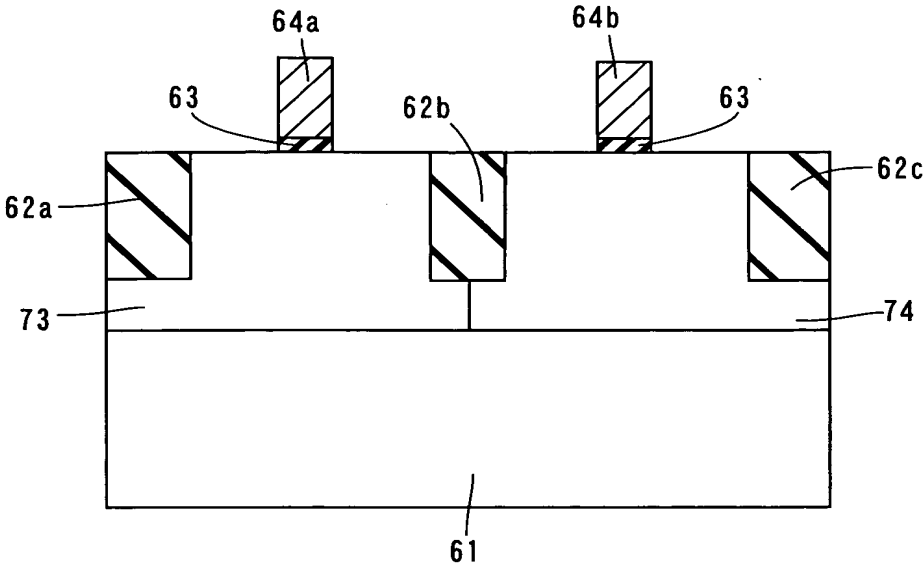
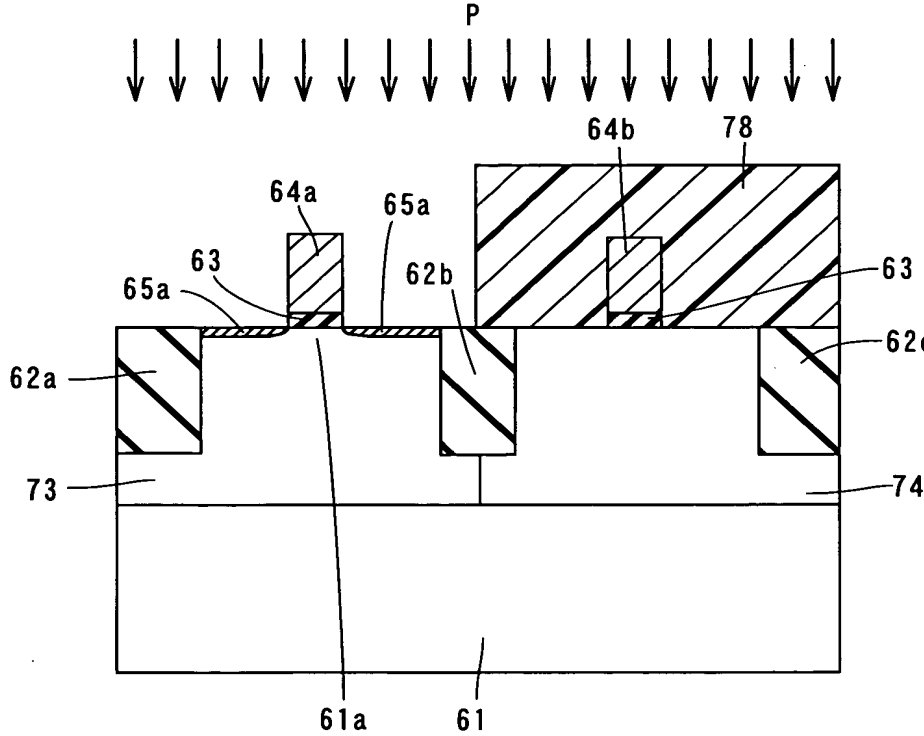


FIG.48





A cross-sectional view of a semiconductor device. A top layer 79 is shown with a downward force  $F$  applied. Below it is a middle layer 63, which contains two rectangular features 64a and 64b. The middle layer 63 is supported by a bottom layer 74. The bottom layer 74 has a central region 61 and side regions 65a and 75a. The middle layer 63 has a central region 62b and side regions 62a and 62c. A layer 73 is located between the middle layer 63 and the bottom layer 74. The bottom layer 74 is divided into regions 65a, 61a, 65a, 61, 75a, 61b, and 75a.

[illegible]

This cross-sectional view shows the device structure in a second direction B. It features a substrate 73 with a top layer 74. A central region 61 is defined by a series of vertical lines. On the left, a structure 62a is shown, and on the right, a structure 62c is shown. A central structure 62b is also present. The top surface is divided into regions 65, 66, 64a, 64b, and 63. Arrows indicate the direction of light or signal passing through the device.

FIG.53

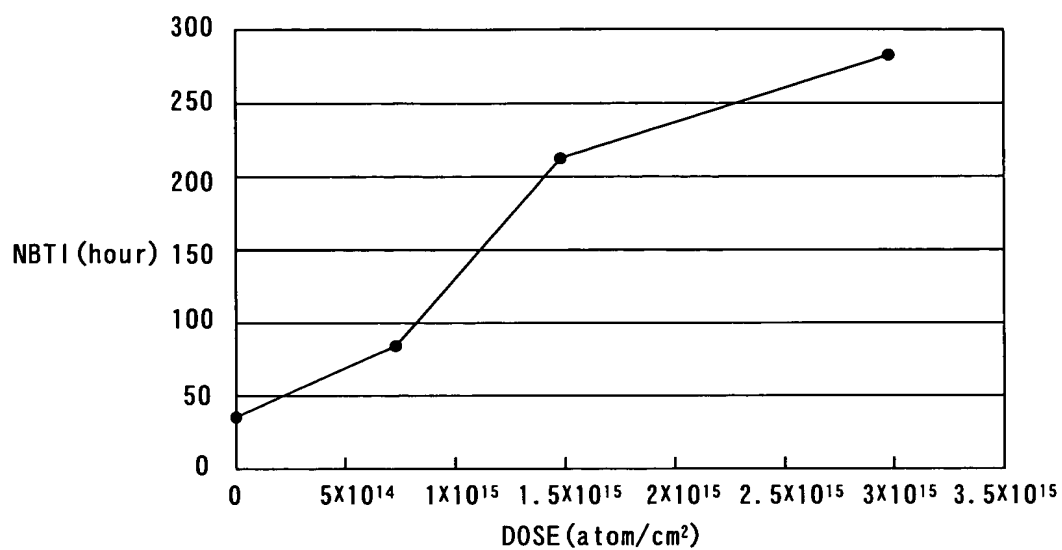


FIG.54

